Field Effect Transistors

MEASURE THE CHARACTERISTICS OF A FIELD EFFECT TRANSISTOR

- **Measure the drain current as a function of the drain-source voltage for various gate voltages.**
- **Confirm the shape of the characteristic when the drain current is governed by the drain-source voltage and the gate voltage.**

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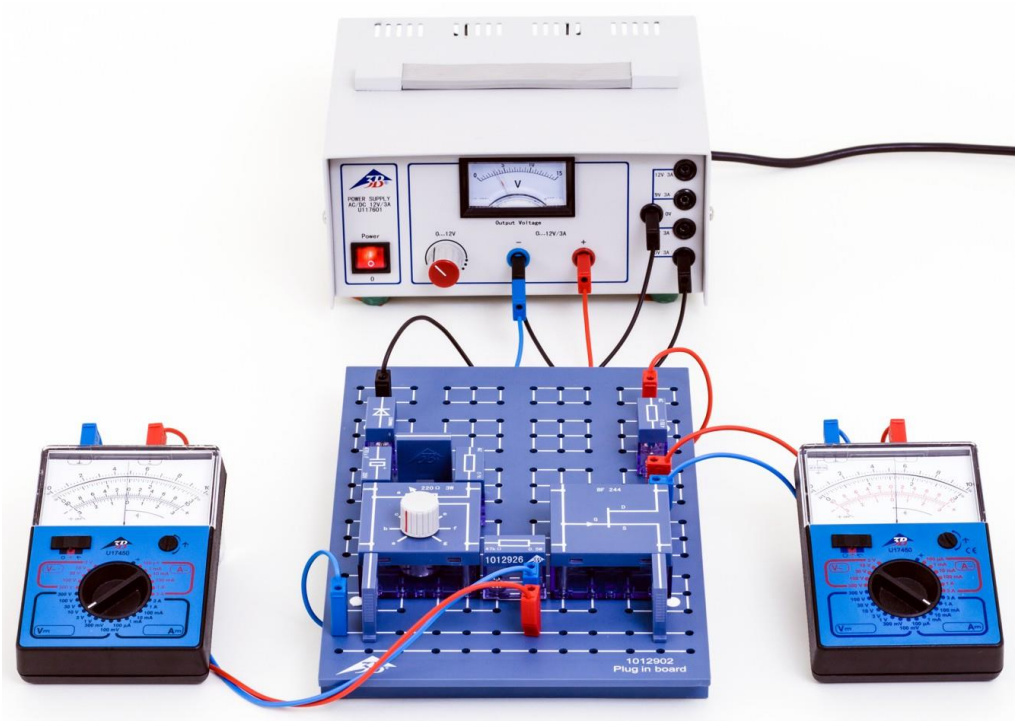

Fig. 1: Experiment set-up

GENERAL PRINCIPLES

A field effect transistor (FET) is a semiconductor component in which electric current passes through a channel and is controlled by an electric field acting perpendicular to the channel.

FETs have three contacts, called source (S), drain (D) and gate (G) due to their respective functions. The channel comprises a conductive link between the source and the drain. If a voltage U_{DS} is applied between source and drain, a drain current I_D flows in the channel. The current is carried by carriers of only one polarity (unipolar transistors), i.e. electrons for an n-doped semiconductor channel and holes in a p-doped channel. The cross-section or the conductivity of the channel is controlled by the electric field perpendicular to the channel. To create this field, a gate voltage U_{GS} is applied between the source and gate. The gate electrode is isolated from the channel by means of a reverse-biased pn junction or by an extra insulating layer (IGFET, MISFET, MOSFET). For insulated gate FETs the cross section of the channel is controlled by the expansion of the space-charge region of the junction, which is itself controlled by the perpendicular field.

In order to ensure that the pn junction is always reverse-biased, i.e. specifically to make sure that there is no current at the gate, the gate voltage U_{GS} and the drain-source voltage U_{DS} must meet the following condition for an n-channel FET

(1a) $U_{GS} \leq 0, U_{DS} \geq 0$

and the following for a p-channel FET

(1b) $U_{GS} \geq 0, U_{DS} \geq 0$.

If the absolute value of the drain-source voltage $|U_{DS}|$ is small, the FET acts like an ohmic resistor with a correspondingly linear characteristic. As $|U_{DS}|$ increases, the channel is restricted in size because the reverse-bias voltage between the gate and the channel increases in the direction of the drain. The space-charge region near the drain is wider than that near the source, meaning that the channel is narrower near the drain than it is near the source. At a specific voltage where $U_{DS} = U_p$ the width of the channel becomes zero and the drain current no longer increases even though the drain-source voltage is increased. The characteristic passes out of its ohmic region into a region of saturation.

The extent of the space-charge region and therefore the size of the channel can be controlled by means of the gate voltage. As long as the gate voltage is non-zero, the channel can undergo additional constriction, making the drain-source current smaller and, in particular, the saturation current lower. The channel remains blocked irrespective of the drain-source voltage U_{DS} when $|U_{GS}| \geq |U_p|$.

The experiment involves measuring drain current I_D as a function of drain-source voltage U_{DS} for various gate voltages U_{GS}.

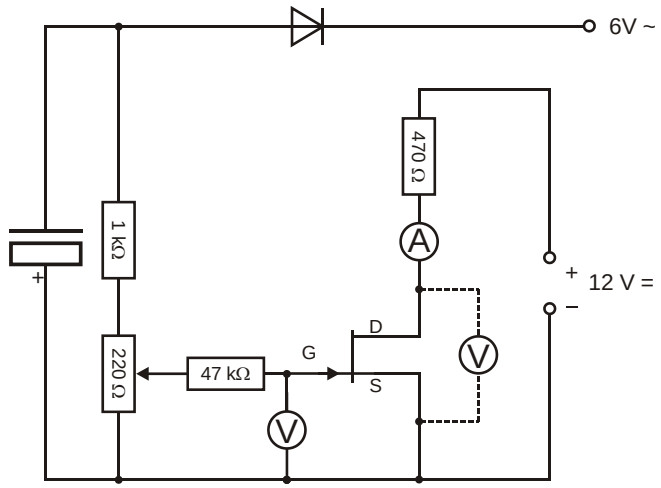

Fig. 2: Sketch of circuit.

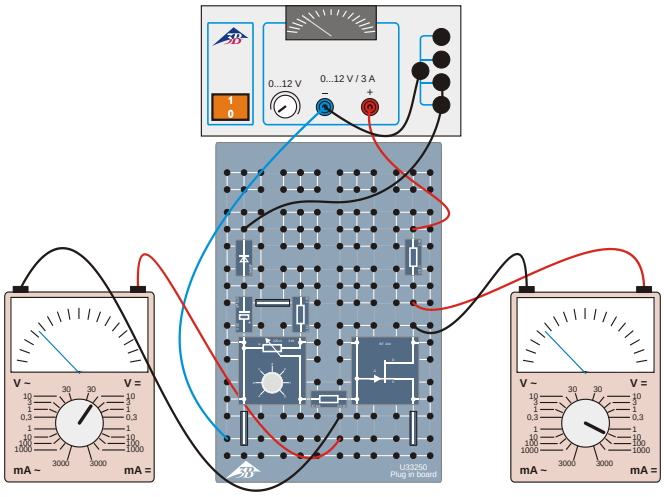

Fig. 3: Voltmeter between gate and source.

LIST OF EQUIPMENT

1	Plug-In Board for Components	1012902 (U33250)
1	Set of 10 Jumpers, P2W19	1012985 (U333093)
1	Resistor, 1 kΩ, 2 W, P2W19	1012916 (U333024)
1	Resistor, 470 Ω, 2 W, P2W19	1012914 (U333022)
1	Resistor, 47 kΩ, 0,5 W, P2W19	1012926 (U333034)
1	Capacitor, 470 µF, 16 V, P2W19	1012960 (U333068)
1	FET Transistor, BF 244, P4W50	1012978 (U333086)
1	Silicon Diode,1N 4007, P2W19	1012964 (U333072)
1	Potentiometer, 220 Ω, 3 W, P4W50	1012934 (U333042)
1	AC/DC Power Supply, 0…12 V/3 A @230 V	1002776 (U117601-230)
or		
1	AC/DC Power Supply, 0…12 V/3 A @115 V	1002775 (U117601-115)
2	Escola 30 Analogue Multimeter	1013526 (U8557330)
1	Set of 15 Experiment Leads, 75 cm, 1 mm²	1002840 (U13800)

SET-UP AND EXPERIMENT PROCEDURE

- Set up the circuit as shown in Fig. 2 and Fig. 3. Make sure you get the correct polarity for the silicon diode and capacitor.
- Initially connect up the analogue multimeter so that you can measure the voltage between the gate and source. Connect the negative pole to the gate (Fig 3).
- Set up a measuring range of 10 V DC on the voltmeter and a range of 10 mA DC on the ammeter.
- Turn on the power supply and set the voltage to 0 V DC.
- Turn the potentiometer knob to position "a" to set up a gate voltage U_{GS} of 0 V.

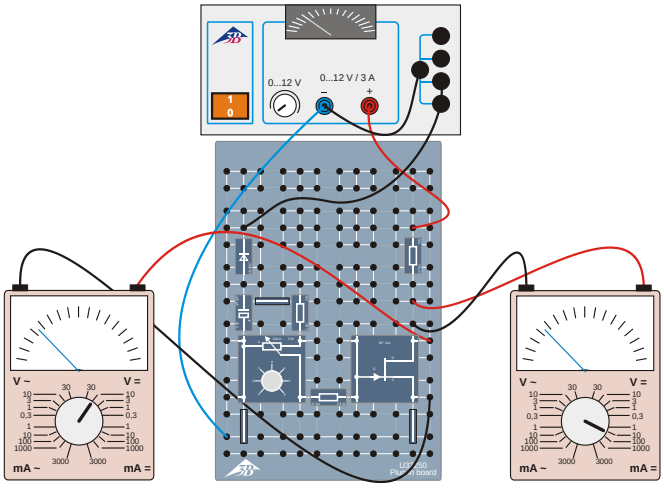

Fig. 4: Voltmeter between drain and source.

- Now connect the voltmeter between the drain and the source. Connect the positive pole to the drain (Fig. 4).
- Increase the voltage from the power supply until the drain-source voltage shown on the voltmeter is U_{DS} = 0.25 V. Enter the value into Table 1.
- Read off the drain current I_D from the ammeter and enter the value into Table 1.
- Set up a drain-source voltage U_{DS} = 0.5 V and enter the value into Table 1.
- Read off the drain current I_D from the ammeter and enter the value into Table 1.
- Increase the drain-source voltage U_{DS} in steps of 0.5 V. For each step, read off the drain current I_D from the ammeter and enter the values into Table 1.
- Turn the voltage back to 0 V on the power supply.
- Set up gate voltages U_{GS} = -0.5 V, -1 V and -1.5 V, repeat the above set of measurements for each of these voltages, then enter the drain-source voltages and corresponding drain currents into Table 1.

SAMPLE MEASUREMENT

Table 1: Configured drain-source voltages with corresponding measurements of drain current for various gate voltages.

U_{DS} / V	I_D / mA			
	U_{GS} = 0.0 V	U_{GS} = -0.5 V	U_{GS} = -1.0 V	U_{GS} = -1.5 V
0.00	0.00	0.00	0.00	0.00
0.25	1.20	0.90	0.65	0.40
0.50	2.40	1.90	1.35	0.80
1.00	4.30	3.40	2.30	1.25
1.50	5.70	4.20	2.70	1.45
2.00	6.50	4.60	2.95	1.50
2.50	6.90	4.90	3.05	1.55
3.00	7.10	5.00	3.15	1.60
3.50	7.30	5.10	3.20	1.65
4.00	7.40	5.15	3.25	1.65
4.50	7.45	5.20	3.30	1.65
5.00	7.50	5.25	3.30	1.65

EVALUATION

- Plot a graph of I_D against U_{DS} for each of the various gate voltages (Fig. 5)

The expected shape of the characteristics arising from controlling the drain current by means of the drain-source voltage and gate voltage is confirmed to be as described.

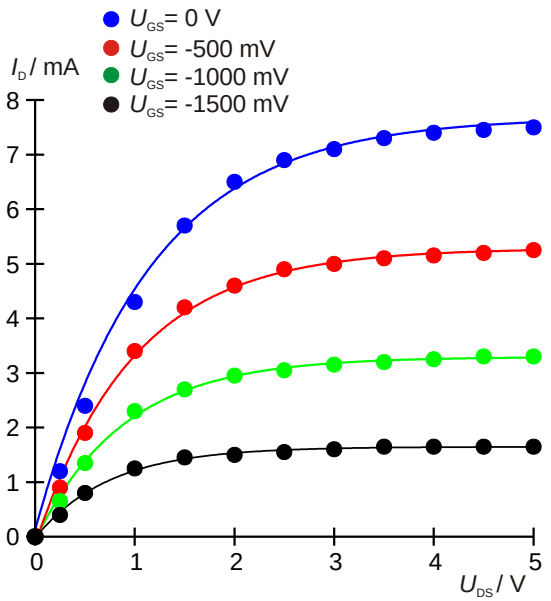

Fig. 5: Characteristic curves for a field effect transistor at various gate voltages.