

## EXPERIMENT PROCEDURE

- Measure the drain voltage as a function of the drain current for various voltages at the gate.

## OBJECTIVES

Measure the characteristics of a field effect transistor.

## SUMMARY

A field effect transistor (FET) is a semiconductor component in which electric current passes through a channel and is controlled by an electric field acting perpendicular to the channel. FETs have three contacts, called source, drain and gate due to their respective functions. If a voltage is applied between the source and the drain, then a drain current flows between the two. For small voltages between the drain and source, an FET acts like a simple ohmic resistor with a correspondingly linear characteristic. As the source-drain voltage increases, the channel becomes restricted and eventually is cut off entirely. The characteristic then enters an area of saturation. When the gate voltage is non-zero, the saturation value of the drain current decreases.

## REQUIRED APPARATUS

Quantity	Description	Number
1	Plug-In Board for Components	1012902
1	Set of 10 Jumpers, P2W19	1012985
1	Resistor 1 k $\Omega$ , 2 W, P2W19	1012916
1	Resistor 470 $\Omega$ , 2 W, P2W19	1012914
1	Resistor 47 k $\Omega$ , 0.5 W, P2W19	1012926
1	Capacitor 470 $\mu$ F, 16 V, P2W19	1012960
1	FET Transistor, BF 244, P4W50	1012978
1	Silicon Diode, 1N 4007, P2W19	1012964
1	Potentiometer 220 $\Omega$ , 3 W, P4W50	1012934
1	AC/DC Power Supply 0 – 12 V, 3 A (230 V, 50/60 Hz)	1002776 or
	AC/DC Power Supply 0 – 12 V, 3 A (115 V, 50/60 Hz)	1002775
2	Analogue Multimeter AM50	1003073
1	Set of 15 Experiment Leads, 75 cm 1 mm <sup>2</sup>	1002840

# 2

## BASIC PRINCIPLES

A field effect transistor (FET) is a semiconductor component in which electric current passes through a channel and is controlled by an electric field acting perpendicular to the channel.

FETs have three contacts, called source (S), drain (D) and gate (G) due to their respective functions. The channel comprises a conductive link between the source and the drain. If a voltage  $U_{DS}$  is applied between source and drain, a drain current  $I_D$  flows in the channel. The current is carried by carriers of only one polarity (unipolar transistors), i.e. electrons for an n-doped semiconductor channel and holes in a p-doped channel. The cross-section or the conductivity of the channel is controlled by the electric field perpendicular to the channel. To create this field, a gate voltage  $U_{GS}$  is applied between the source and gate. The gate electrode is isolated from the channel by means of a reverse-biased pn junction or by an extra insulating layer (IGFET, MISFET, MOSFET). For insulated gate FETs the cross section of the channel is controlled by the expansion of the space-charge region of the junction, which is itself controlled by the perpendicular field. In order to ensure that the pn junction is always reverse-biased, i.e. specifically to make sure that there is no current at the gate, the gate voltage  $U_{GS}$  and the drain-source voltage  $U_{DS}$  must meet the following condition for an n-channel FET

$$(1a) \quad U_{GS} \leq 0, U_{DS} \geq 0$$

and the following for a p-channel FET

$$(1b) \quad U_{GS} \geq 0, U_{DS} \geq 0.$$

If the absolute value of the drain-source voltage  $|U_{DS}|$  is small, the FET acts like an ohmic resistor with a correspondingly linear characteristic. As  $|U_{DS}|$  increases, the channel is restricted in size because the reverse-bias voltage between the gate and the channel increases in the direction of the drain. The space-charge region near the drain is wider than that near the source, meaning that the channel is narrower near the drain than it is near the source. At a specific voltage where  $U_{DS} = U_p$  the width of the channel becomes zero and the drain current no longer increases even though the drain-source voltage is increased. The characteristic passes out of its ohmic region into a region of saturation.

The extent of the space-charge region and therefore the size of the channel can be controlled by means of the gate voltage. As long as the gate voltage is non-zero, the channel can undergo additional constriction, making the drain-source current smaller and, in particular, the saturation current lower. The channel remains blocked irrespective of the drain-source voltage  $U_{DS}$  when  $|U_{GS}| \geq |U_p|$ .

The experiment involves measuring drain current  $I_D$  as a function of drain-source voltage  $U_{DS}$  for various gate voltages  $U_{GS}$ .

## EVALUATION

The measurements are plotted on a graph of  $I_D$  against  $U_{DS}$  for various values of the gate voltage  $U_{GS}$  (Fig. 1). This should verify the shape of the characteristic showing how the drain current is controlled by the drain-source voltage and gate voltage.

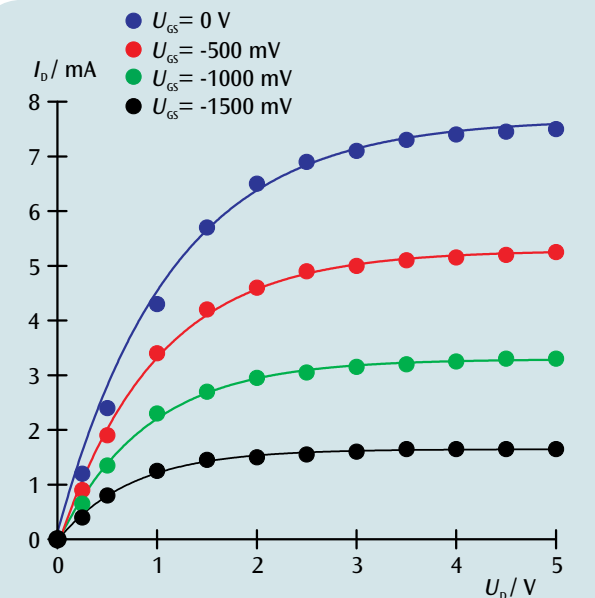


Fig. 1: Characteristic curve for FET with gate voltages 0 V (blue), -0.5 V (red), -1 V (green) and -1.5 V (turquoise)